WHAT IS CLAIMED IS:

1. μ-law-to-A-law translating equipment, comprising:

a timing pulse generator that generates a reference frame pulse;

a μ-law signal receiving circuit that receives a μ-law PCM signal and outputs parallel μ-law PCM signals according to a reference frame pulse;

a multiplexer that time-division multiplexes plural parallel μ-law PCM signals and outputs a time-division multiplexed μ-law PCM signal;

a μ-law-to-A-law converter that converts the time-division multiplexed μ-law PCM signal to a time-division multiplexed A-law PCM signal;

a demultiplexer that demultiplexes the time-division multiplexed A-law PCM signal and outputs plural parallel A-law PCM signals; and

an A-law signal output circuit that receives the parallel A-law PCM signals and outputs a serial A-law PCM signal.

2. μ-law-to-A-law translating equipment according to Claim 1, comprising:

respective plural and the same number of μ-law signal receiving circuits and A-law signal output circuits.

3. μ-law-to-A-law translating equipment according to Claim 1, wherein:

the μ-law signal receiving circuit comprises:

a line receiver that converts a μ-law PCM signal from

bipolar to unipolar and outputs a unipolar μ-law signal;

a frame buffer that temporarily stores the unipolar μ-law signal;

a frame detector that detects the frame leading part of the unipolar μ-law signal and generates an address reset pulse synchronized with the frame leading position for writing to the frame buffer;

a frame position comparator that measures the time lag in a position of a reference frame pulse and the address reset pulse for writing to the frame buffer and generates an address reset pulse for reading from the frame buffer; and

a serial-parallel converter that converts and outputs a serial μ-law PCM signal read from the frame buffer to parallel μ-law PCM signals.

4. μ-law-to-A-law translating equipment according to Claim 1, wherein:

the A-law signal output circuit comprises:

a parallel-serial converter that converts parallel A-law PCM signals to a serial A-law PCM signal; and

a frame inserter that inserts a frame bit into the serial A-law PCM signal.

5. μ-law-to-A-law translating equipment according to Claim 4, wherein:

the frame inserter inserts a frame bit according to a reference frame pulse.

6. μ-law-to-A-law translating equipment according to Claim 4, wherein:

the A-law signal output circuit further comprises:

a line driver that outputs a serial A-law PCM signal at a predetermined output amplitude level.

7. A-law-to-μ-law translating equipment, comprising:

a timing pulse generator that generates a reference frame pulse;

an A-law signal receiving circuit that receives an A-law PCM signal and outputs parallel A-law PCM signals according to a reference frame pulse;

a multiplexer that time-division multiplexes plural parallel A-law PCM signals and outputs a time-division multiplexed A-law PCM signal;

an A-law-to-μ-law converter that converts the time-division multiplexed A-law PCM signal to a time-division multiplexed μ-law PCM signal;

a demultiplexer that demultiplexes the time-division multiplexed μ-law PCM signal and outputs plural parallel μ-law PCM signals; and

a μ-law signal output circuit that receives parallel μ-law PCM signals and outputs a serial μ-law PCM signal.

8. A-law-to-μ-law translating equipment according to Claim 7, comprising:

respective plural and the same number of A-law signal receiving circuits and μ-law signal output circuits.

9. A-law-to-μ-law translating equipment according to Claim 7, wherein:

the A-law signal receiving circuit comprises:

a line receiver that converts an A-law PCM signal from bipolar to unipolar and outputs a unipolar A-law signal;

a frame buffer that temporarily stores the unipolar A-law signal;

a frame detector that detects the frame leading part of the unipolar A-law signal and generates an address reset pulse synchronized with the frame leading position for writing to the frame buffer;

a frame position comparator that measures the time lag in a position of a reference frame pulse and the address reset pulse for writing to the frame buffer and generates an address reset pulse for reading from the frame buffer; and

a serial-parallel converter that converts a serial A-law PCM signal read from the frame buffer to parallel A-law PCM signals.

10. A-law-to-μ-law translating equipment according to Claim 7, wherein:

the μ-law signal output circuit comprises:

a parallel-serial converter that converts parallel μ-law PCM signals to a serial μ-law PCM signal; and

a frame inserter that inserts a frame bit into the serial μ-law PCM signal.

11. A-law-to-μ-law translating equipment according to Claim

10, wherein:

the frame inserter adds a frame bit to the serial μ-law PCM signal according to a reference frame pulse.

12. A-law-to-μ-law translating equipment according to Claim 10, wherein:

the μ-law signal output circuit further comprises:

a line driver that outputs a serial μ-law PCM signal at a predetermined output amplitude level.

13. μ-law-to-A-law and A-law-to-μ-law translating equipment, comprising:

a timing pulse generator that generates a reference frame pulse;

μ-law-to-A-law translating equipment; and

A-law-to-μ-law translating equipment, wherein:

the μ-law-to-A-law translating equipment comprises:

a μ-law signal receiving circuit that receives a μ-law PCM signal and outputs parallel μ-law PCM signals according to a reference frame pulse;

a multiplexer that time-division multiplexes plural parallel μ-law PCM signals and outputs a time-division multiplexed μ-law PCM signal;

a μ-law-to-A-law converter that converts the time-division multiplexed μ-law PCM signal to a time-division multiplexed A-law PCM signal;

a demultiplexer that demultiplexes the time-division multiplexed A-law PCM signal and outputs plural parallel A-

law PCM signals;

an A-law signal output circuit that receives the parallel A-law PCM signals and outputs a serial A-law PCM signal; and

the A-law-to-μ-law translating equipment comprises:

an A-law signal receiving circuit that receives an A-law PCM signal and outputs parallel A-law PCM signals according to a reference frame pulse;

a multiplexer that time-division multiplexes plural parallel A-law PCM signals and outputs a time-division multiplexed A-law PCM signal;

an A-law-to-μ-law converter that converts the time-division multiplexed A-law PCM signal to a time-division multiplexed μ-law PCM signal;

a demultiplexer that demultiplexes the time-division multiplexed μ-law PCM signal and outputs plural parallel μ-law PCM signals; and

a μ-law signal output circuit that receives the parallel μ-law PCM signals and outputs a serial μ-law PCM signal.

14. μ-law-to-A-law and A-law-to-μ-law translating equipment according to Claim 13, wherein:

the μ-law-to-A-law translating equipment comprises respective plural and the same number of μ-law signal receiving circuits and A-law signal output circuits; and

the A-law-to-μ-law translating equipment comprises respective plural and the same number of A-law signal receiving circuits and μ-law signal output circuits.